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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.
09/148,392	09/04/98	BAEZ	F 042390.P5512

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THINH V NGUYEN
BLAKELY SOKOLOFF TAYLOR & ZAFMAN
12400 WILSHIRE BOULEVARD
7TH FLOOR
LOS ANGELES CA 90025

EXAMINER	
THOMSON, W	
ART UNIT	PAPER NUMBER
2123	

DATE MAILED: 04/24/01

Please find below and/or attached an Office communication concerning this application or proceeding.

Commissioner of Patents and Trademarks

Office Action Summary

Application No.	Applicant(s)
09/148,392	Baez
Examiner	**Art Unit**
William Thomson	2123

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136 (a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1) ☒ Responsive to communication(s) filed on *Apr 9, 2001* .

2a) ☐ This action is **FINAL.** 2b) ☒ This action is non-final.

3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11; 453 O.G. 213.

Disposition of Claims

4) ☒ Claim(s) *1-20 and 22-27* is/are pending in the application.

4a) Of the above, claim(s) _____ is/are withdrawn from consideration.

5) ☐ Claim(s) _____ is/are allowed.

6) ☒ Claim(s) *1-20 and 22-27* is/are rejected.

7) ☐ Claim(s) _____ is/are objected to.

8) ☐ Claims _____ are subject to restriction and/or election requirement.

Application Papers

9) ☐ The specification is objected to by the Examiner.

10) ☐ The drawing(s) filed on _____ is/are objected to by the Examiner.

11) ☐ The proposed drawing correction filed on _____ is: a) ☐ approved b) ☐ disapproved.

12) ☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. § 119

13) ☐ Acknowledgement is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d).

a) ☐ All b) ☐ Some* c) ☐ None of:

1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

*See the attached detailed Office action for a list of the certified copies not received.

14) ☐ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. § 119(e).

Attachment(s)

15) ☐ Notice of References Cited (PTO-892)

16) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)

17) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s). _____

18) ☐ Interview Summary (PTO-413) Paper No(s). _____

19) ☐ Notice of Informal Patent Application (PTO-152)

20) ☐ Other:

DETAILED ACTION

Continued Prosecution Application

1. The request filed on March 20, 2001 for a Continued Prosecution Application (CPA) under 37 CFR 1.53(d) based on parent Application No. 09/148,392 is acceptable and a CPA has been established. An action on the CPA follows.

2. Claims 1-20, and 22-27 have been submitted for examination. Claims have been amended. Claims 1-20, and 22-27 have been examined and rejected.

TITLE

3. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed. The title is of a generic nature drawn to a family of systems and not to the applicant's specific invention. **Amendment to the title has been entered, yet does not remedy the deficiency.**

ABSTRACT

4. Applicant is reminded of the proper content of an abstract of the disclosure.

A patent abstract is a concise statement of the technical disclosure of the patent and *should include that which is new in the art to which the invention pertains*. If the patent is of a basic nature, the entire technical disclosure may be new in the art, and the abstract should be directed to the entire disclosure. If the patent is in the nature of an improvement in an old apparatus, process, product, or composition, *the abstract should include the technical disclosure of the improvement*. In certain patents, particularly those for compounds and compositions, wherein the process for making and/or the use thereof are not obvious, the abstract should set

Parameter Function. Describes the variation of one parameter as a function of another parameter. Each circuit is characterized by a parameter function. The relationship between the design constraints and the optimizing parameters. *Applicant's specification*

Design Constraints: A constraint set including constraint parameters which are parameters that must be met. A **constraint parameter** is the propagation delay and an **optimizing parameter** is the power consumption. Alternately the propagation delay is the optimizing parameter and the power consumption is the constraint parameter. *Applicant's specification*

Preamble of the Claims

The preamble of the claims presented for examination have not been given patentable weight. Examiner notes the Applicant's have amended an addition phrase "comprising" into the claims. Appropriate weight is given to limitations recited in the body of the claim that are needed for the purpose of antecedence. "A mere statement of purpose or intended use in the preamble of a claim need not be considered in finding anticipation; however, it must be considered if the language of a preamble is necessary to give meaning to the claim" *Diversitech Corp. v. Century Steps, Inc., 7 USPQ2d 1315 (Fed. Cir. 1988); In re Stencel, 4 USPQ2d 1071 (Fed. Cir. 1987)*

Response to Arguments

7. Applicant's arguments filed April, 9, 2001 have been fully considered. Applicant's arguments with respect to claims 1-20, and 22-27 have been considered. This response has been necessitated by Applicant's amendments. Applicant's arguments regarding Sarin and Jyu et al. and Roethig(145) and Breid are not persuasive and the prior art rejection directed to claims 1-20, and 22-27 stands.

Specific Response to Arguments and Amendments

Applicants have amended the claims 1, 11 and 22 to include the following limitations: selecting initial design points for the parameter functions to satisfy the design contraints; and selecting new design points for the parameter functions to optimize design parametes within the design constraints., which do not provide limitations not explicitely and inherently in all designe and redesign modelers. The prior art asserted works in the same fashion.

Unfortunately, all the prior art citations specifically disclose the use of the same methodology as Applicant's have claimed as novel. Sarin and Jyu et al. and Roethig(145) and Breid teach the optimizing and modeling approach. Applicants failed to claim the operational and function differences for optimizing the circuit design and therefore the claims are encompassed by the teachings within Sarin and Jyu et al. and Roethig(145) and Breid. Specifically, Sarin and Jyu et al. and Roethig(145) and Breid explicitly teach a **constraint parameter** that is the propagation delay and an **optimizing parameter** that is the power consumption. Alternately the propagation delay is the optimizing parameter and the power consumption is the constraint parameter. Further,

these relationships are represented in a parameter function that associates the two (or more) parameters for optimizing the circuit(s). Subsystems are transistors in a gate array or sub combinations of the circuits within a larger circuit with interrelated parameters for design, simulation and optimizations.

Furthermore, Applicants' arguments amount to a general allegation that the claims define a patentable invention without specifically pointing out how the language of the claims patentably distinguishes them from the references. Though an attempt at determining a distinction was proffered, the citation was not meaningful. Applicants have responded by selective interpretation and selective viewing without providing a proper analysis as to the points of distinction. Sarin and Jyu et al. and Roethig(145) and Breid provide for the re-designing and optimizing of designs for multiple circuit models and characteristics.

Moreover, Applicant's arguments do not clearly point out the patentable novelty which he or she thinks the claims present in view of the state of the art disclosed by the references cited. Applicant's have not provided *any* effective argument as to any limitations that might be within their application and that might be distinguishable over the prior art teachings of the Sarin and Jyu et al. and Roethig(145) and Breid. Applicant's invention, as claimed, is clearly anticipated by the entire teaching of Sarin and Jyu et al. and Roethig(145) and Breid and the prior art of record.

Applicant is solving the same problem with the same technology in the same manner as Sarin and Jyu et al. and Roethig(145) and Breid. There is no inventive step when all that is claimed is that which is well known and inherent in the prior art teachings. Applicant's invention

and Sarin and Jyu et al. and Roethig(145) and Breid perform the same functions and operations with the same equipment. Both products allow users to design, model, simulate and optimize based on parameter function corresponding to each circuit with iterative operations.

Applicant has not provided any effective argument as to any patentable distinction, improvement or unexpected result that might occur over the prior art teachings when Applicant's method of handling modeling and optimizing for circuits than that which is built into the Sarin and Jyu et al. and Roethig(145) and Breid. Applicants are using the well known methodology to effect designs within a circuit framework. The engineer using a simulation-modeler-Optimizer will always have design constraints built into the model. This includes setting two parameters against one another to yield operational constraints that are used to optimize the layout. This is merely using the well known tool of the trade for its specific purpose. The courts have held that "A reference anticipates a claim if it discloses the claimed invention such that a skilled artisan could take its teachings in combination with his own knowledge of the particular art and be in possession of the invention.". *In re Graves, 36 USPQ2d 1697 (Fed. Cir. 1995); In re Sase, 207 USPQ 107 (CCPA 1980); In re Samour, 197 USPQ 1 (CCPA 1978).*

Applicant is currently claiming a system which uses timing or propagation delays and power parameters to optimize transistor sizing. The relationships between these two parameters and the sizing of a circuit are well known in the art. The use of a computer system to optimize the layout and sizing of the circuit based on these parameters is just as old in the art. Graphical

and curve trace methodologies for optimizations that cover applicant's claimed invention go back for many years.

Claim Rejections - 35 U.S.C. § 102

8. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless --
> (a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
>
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

9. Claims 1-20, and 22-27 are rejected under 35 U.S.C. 102(e) as being clearly anticipated by Sarin or Jyu et al. or Jones et al. (288) or Roethig (145) and rejected under 102(a) as being clearly anticipated by Roethig(145) and rejected under 102(b) as being clearly anticipated by Breid.

Taking claim 1, for example, Sarin and Jyu et al. and Jones et al. (288) and Roethig(145) and Breid disclose:

(Sarin: Abstract, Figures 1-4, 7, 8, 10, 11, 12, col. 2, lines 14 et seq., col. 4, lines 21 et seq., , Verilog and Powergate; Breid: Abstract, Figures 2-4, flowcharts in figures 5 and 6, col. 6, lines 20 et seq.; Jyu et al.: Abstract, Figures 3, 4A-4B, circuit areas 500 and 502, flowcharts in figures 6, 6A-6E, note power/transistor parameter records 702 and 704, 706 and 708, see figure 7C, 8-10, flowcharts in figures 11A and 11B, 11C-15 (code), 16-24, region of interest in figure 25, figure

26, figures 27 and 28, col. 6, lines 6 et seq., design goals, col. 10, lines 52 et seq., POWERMILL, col. 18, lines 28 et seq.; Roethig: Abstract, Figures 4, 6, 5, 7A & 7B, 9, 10, 11, 12, 13, 16-18, col. 4, lines 42 et seq.; Jones et al.: Abstract, Figures 3, 4 and 5, col. 3, lines 29 et seq.)

A method for determining optimal values of design parameters of a subsystem comprising a plurality of circuits, the method comprising:

creating parameter functions for a plurality of circuits in a subsystem, the subsystem having design constraints, each one of the parameter functions corresponding to each one of the circuits, the corresponding circuits, the parameter functions representing a relationship among the design parameters;

selecting initial design points for the parameter functions to satisfy the design contraints; and

selecting new design points for the parameter functions to optimize design parametes within the design constraints.

As to claim 2, the method of claim 1, wherein the creating the parameter functions comprises:

configuring each circuit of the plurality of circuits and generating values of design parameters for each circuit according to the configuration circuit, the values providing the parameter functions are discloses throughout Sarin and Jyu et al. and Jones et al. (288) and Roethig (145) and Breid.(Sarin: Abstract, Figures 1-4, 7, 8, 10, 11, 12, col. 2, lines 14 et seq., col. 4, lines 21 et seq., , Verilog and Powergate; Breid: Abstract, Figures 2-4, flowcharts in

figures 5 and 6, col. 6, lines 20 et seq.; Jyu et al.: Abstract, Figures 3, 4A-4B, circuit areas 500 and 502, flowcharts in figures 6, 6A-6E, note power/transistor parameter records 702 and 704, 706 and 708, see figure 7C, 8-10, flowcharts in figures 11A and 11B, 11C-15 (code), 16-24, region of interest in figure 25, figure 26, figures 27 and 28, col. 6, lines 6 et seq., design goals, col. 10, lines 52 et seq., POWERMILL, col. 18, lines 28 et seq.; Roethig: Abstract, Figures 4, 6, 5, 7A & 7B, 9, 10, 11, 12, 13, 16-18, col. 4, lines 42 et seq.; Jones et al.: Abstract, Figures 3, 4 and 5, col. 3, lines 29 et seq.)

As to claim 3, the method of claim 2, wherein the design parameters include constraint and optimizing sets, the constraint set including constraint parameters having values selectable to meet the design constraints, the optimizing set including optimizing parameters having values to be optimized are disclosed throughout Sarin and Jyu et al. and Jones et al. (288) and Roethig(145) and Breid. (Sarin: Abstract, Figures 1-4, 7, 8, 10, 11, 12, col. 2, lines 14 et seq., col. 4, lines 21 et seq., , Verilog and Powergate; Breid: Abstract, Figures 2-4, flowcharts in figures 5 and 6, col. 6, lines 20 et seq.; Jyu et al.: Abstract, Figures 3, 4A-4B, circuit areas 500 and 502, flowcharts in figures 6, 6A-6E, note power/transistor parameter records 702 and 704, 706 and 708, see figure 7C, 8-10, flowcharts in figures 11A and 11B, 11C-15 (code), 16-24, region of interest in figure 25, figure 26, figures 27 and 28, col. 6, lines 6 et seq., design goals, col. 10, lines 52 et seq., POWERMILL, col. 18, lines 28 et seq.; Roethig: Abstract, Figures 4, 6, 5, 7A & 7B, 9, 10, 11, 12, 13, 16-18, col. 4, lines 42 et seq.; Jones et al.: Abstract, Figures 3, 4 and 5, col. 3, lines 29 et seq.)

As to claim 4, the method of claim 3, wherein optimizing comprises:

selecting values of the constraint parameters to meet the design constraints;

determining values of the optimizing parameters corresponding to the selected values of the constraint parameters based on the parameter functions; and

iterating the selection of values and determining of values steps until values of the optimizing parameters are within a predetermined optimal range are disclosed throughout Sarin and Jyu et al. and Jones et al. (288) and Roethig(145) and Breid.(Sarin: Abstract, Figures 1-4, 7, 8, 10, 11, 12, col. 2, lines 14 et seq., col. 4, lines 21 et seq., , Verilog and Powergate; Breid: Abstract, Figures 2-4, flowcharts in figures 5 and 6, col. 6, lines 20 et seq.; Jyu et al.: Abstract, Figures 3, 4A-4B, circuit areas 500 and 502, flowcharts in figures 6, 6A-6E, note power/transistor parameter records 702 and 704, 706 and 708, see figure 7C, 8-10, flowcharts in figures 11A and 11B, 11C-15 (code), 16-24, region of interest in figure 25, figure 26, figures 27 and 28, col. 6, lines 6 et seq., design goals, col. 10, lines 52 et seq., POWERMILL, col. 18, lines 28 et seq.; Roethig: Abstract, Figures 4, 6, 5, 7A & 7B, 9, 10, 11, 12, 13, 16-18, col. 4, lines 42 et seq.; Jones et al.: Abstract, Figures 3, 4 and 5, col. 3, lines 29 et seq.)

As to claim 5, the method of claim 3, wherein the constraint parameters include a delay parameter and the optimizing parameters include a power parameter are disclosed throughout Sarin and Jyu et al. and Jones et al. (288) and Roethig (145) and Breid.(Sarin: Abstract, Figures 1-4, 7, 8, 10, 11, 12, col. 2, lines 14 et seq., col. 4, lines 21 et seq., , Verilog and Powergate; Breid: Abstract, Figures 2-4, flowcharts in figures 5 and 6, col. 6, lines 20 et seq.; Jyu et al.:

Abstract, Figures 3, 4A-4B, circuit areas 500 and 502, flowcharts in figures 6, 6A-6E, note power/transistor parameter records 702 and 704, 706 and 708, see figure 7C, 8-10, flowcharts in figures 11A and 11B, 11C-15 (code), 16-24, region of interest in figure 25, figure 26, figures 27 and 28, col. 6, lines 6 et seq., design goals, col. 10, lines 52 et seq., POWERMILL, col. 18, lines 28 et seq.; Roethig: Abstract, Figures 4, 6, 5, 7A & 7B, 9, 10, 11, 12, 13, 16-18, col. 4, lines 42 et seq.; Jones et al.: Abstract, Figures 3, 4 and 5, col. 3, lines 29 et seq.)

As to claim 6, the method of claim 5, wherein the design constraints include a delay constraint are disclosed throughout Sarin and Jyu et al. and Jones et al. (288) and Roethig (145) and Breid.(Sarin: Abstract, Figures 1-4, 7, 8, 10, 11, 12, col. 2, lines 14 et seq., col. 4, lines 21 et seq., , Verilog and Powergate; Breid: Abstract, Figures 2-4, flowcharts in figures 5 and 6, col. 6, lines 20 et seq.; Jyu et al.: Abstract, Figures 3, 4A-4B, circuit areas 500 and 502, flowcharts in figures 6, 6A-6E, note power/transistor parameter records 702 and 704, 706 and 708, see figure 7C, 8-10, flowcharts in figures 11A and 11B, 11C-15 (code), 16-24, region of interest in figure 25, figure 26, figures 27 and 28, col. 6, lines 6 et seq., design goals, col. 10, lines 52 et seq., POWERMILL, col. 18, lines 28 et seq.; Roethig: Abstract, Figures 4, 6, 5, 7A & 7B, 9, 10, 11, 12, 13, 16-18, col. 4, lines 42 et seq.; Jones et al.: Abstract, Figures 3, 4 and 5, col. 3, lines 29 et seq.)

As to claim 7, the method of claim 6, wherein the step of configuring each circuit of the plurality of circuits includes sizing components in each circuit is disclosed throughout Sarin and Jyu et al. and Jones et al. (288) and Roethig (145) and Breid.(Sarin: Abstract, Figures 1-4, 7, 8,

10, 11, 12, col. 2, lines 14 et seq., col. 4, lines 21 et seq., , Verilog and Powergate; Breid: Abstract, Figures 2-4, flowcharts in figures 5 and 6, col. 6, lines 20 et seq.; Jyu et al.: Abstract, Figures 3, 4A-4B, circuit areas 500 and 502, flowcharts in figures 6, 6A-6E, note power/transistor parameter records 702 and 704, 706 and 708, see figure 7C, 8-10, flowcharts in figures 11A and 11B, 11C-15 (code), 16-24, region of interest in figure 25, figure 26, figures 27 and 28, col. 6, lines 6 et seq., design goals, col. 10, lines 52 et seq., POWERMILL, col. 18, lines 28 et seq.; Roethig: Abstract, Figures 4, 6, 5, 7A & 7B, 9, 10, 11, 12, 13, 16-18, col. 4, lines 42 et seq.; Jones et al.: Abstract, Figures 3, 4 and 5, col. 3, lines 29 et seq.)

As to claim 8, the method of claim 6, wherein the step of configuring each circuit of the plurality of circuits includes selecting a design technology for each circuit, the design technology being one of static and dynamic technologies is disclosed throughout Sarin and Jyu et al. and Jones et al. (288) and Roethig (145) and Breid.(Sarin: Abstract, Figures 1-4, 7, 8, 10, 11, 12, col. 2, lines 14 et seq., col. 4, lines 21 et seq., , Verilog and Powergate; Breid: Abstract, Figures 2-4, flowcharts in figures 5 and 6, col. 6, lines 20 et seq.; Jyu et al.: Abstract, Figures 3, 4A-4B, circuit areas 500 and 502, flowcharts in figures 6, 6A-6E, note power/transistor parameter records 702 and 704, 706 and 708, see figure 7C, 8-10, flowcharts in figures 11A and 11B, 11C-15 (code), 16-24, region of interest in figure 25, figure 26, figures 27 and 28, col. 6, lines 6 et seq., design goals, col. 10, lines 52 et seq., POWERMILL, col. 18, lines 28 et seq.; Roethig: Abstract, Figures 4, 6, 5, 7A & 7B, 9, 10, 11, 12, 13, 16-18, col. 4, lines 42 et seq.; Jones et al.: Abstract, Figures 3, 4 and 5, col. 3, lines 29 et seq.)

As to claim 9, the method of claim 7, wherein the generating values of design parameters for each circuit according to the configured circuit, the values providing the parameter functions including generating a circuit netlist representing the configured circuit;

generating a timing file based on the circuit netlist using a circuit critical path;

calculating timing values by using a timing simulator; and

calculating power values by using a power estimator is disclosed throughout Sarin and Jyu et al. and Jones et al. (288) and Roethig (145) and Breid.(Sarin: Abstract, Figures 1-4, 7, 8, 10, 11, 12, col. 2, lines 14 et seq., col. 4, lines 21 et seq., , Verilog and Powergate; Breid: Abstract, Figures 2-4, flowcharts in figures 5 and 6, col. 6, lines 20 et seq.; Jyu et al.: Abstract, Figures 3, 4A-4B, circuit areas 500 and 502, flowcharts in figures 6, 6A-6E, note power/transistor parameter records 702 and 704, 706 and 708, see figure 7C, 8-10, flowcharts in figures 11A and 11B, 11C-15 (code), 16-24, region of interest in figure 25, figure 26, figures 27 and 28, col. 6, lines 6 et seq., design goals, col. 10, lines 52 et seq., POWERMILL, col. 18, lines 28 et seq.; Roethig: Abstract, Figures 4, 6, 5, 7A & 7B, 9, 10, 11, 12, 13, 16-18, col. 4, lines 42 et seq.; Jones et al.: Abstract, Figures 3, 4 and 5, col. 3, lines 29 et seq.)

As to claim 10, the method of claim 8, wherein selecting the new design points comprises:

selecting values of the delay parameter within the delay constraint;

determining values of the power parameter corresponding to the selected values of the delay parameter based on the parameter function; and

iterating the steps of selecting values and determining values until values of the power parameter are within a predetermined optimal range are disclosed throughout Sarin and Jyu et al. and Jones et al. (288) and Roethig (145) and Breid.(Sarin: Abstract, Figures 1-4, 7, 8, 10, 11, 12, col. 2, lines 14 et seq., col. 4, lines 21 et seq., , Verilog and Powergate; Breid: Abstract, Figures 2-4, flowcharts in figures 5 and 6, col. 6, lines 20 et seq.; Jyu et al.: Abstract, Figures 3, 4A-4B, circuit areas 500 and 502, flowcharts in figures 6, 6A-6E, note power/transistor parameter records 702 and 704, 706 and 708, see figure 7C, 8-10, flowcharts in figures 11A and 11B, 11C-15 (code), 16-24, region of interest in figure 25, figure 26, figures 27 and 28, col. 6, lines 6 et seq., design goals, col. 10, lines 52 et seq., POWERMILL, col. 18, lines 28 et seq.; Roethig: Abstract, Figures 4, 6, 5, 7A & 7B, 9, 10, 11, 12, 13, 16-18, col. 4, lines 42 et seq.; Jones et al.: Abstract, Figures 3, 4 and 5, col. 3, lines 29 et seq.)

As for claims 11-20, 22-27 are rejected for the same reasoning as claims 1-10, set forth above, *supra.*. Claims 11-20, 22-27 are equivalent machine readable medium having embodied a computer program for processing by a machine and system claims containing the same limitations and variations of limitations as recited in method claims 1-10 and taught throughout Sarin and Jyu et al. and Jones et al. (288) and Roethig (145) and Breid.(Sarin: Abstract, Figures 1-4, 7, 8, 10, 11, 12, col. 2, lines 14 et seq., col. 4, lines 21 et seq., , Verilog and Powergate; Breid: Abstract, Figures 2-4, flowcharts in figures 5 and 6, col. 6, lines 20 et seq.; Jyu et al.: Abstract, Figures 3, 4A-4B, circuit areas 500 and 502, flowcharts in figures 6, 6A-6E, note power/transistor parameter records 702 and 704, 706 and 708, see figure 7C, 8-10, flowcharts in figures 11A and

11B, 11C-15 (code), 16-24, region of interest in figure 25, figure 26, figures 27 and 28, col. 6, lines 6 et seq., design goals, col. 10, lines 52 et seq., POWERMILL, col. 18, lines 28 et seq.; Roethig: Abstract, Figures 4, 6, 5, 7A & 7B, 9, 10, 11, 12, 13, 16-18, col. 4, lines 42 et seq.; Jones et al.: Abstract, Figures 3, 4 and 5, col. 3, lines 29 et seq.)

10. Any inquiry concerning this communication or earlier communications from the examiner should be directed to William Thomson whose telephone number is (703) 305-0022. The examiner can be usually reached between 9:30 a.m. - 4:00 p.m. Monday thru Friday. Voice mail is checked throughout the day. Please leave a detailed message.

If attempts to reach the Examiner by telephone are unsuccessful, the Examiner's supervisor, Mr. Kevin Teska, can be reached on 704-305-9704. The fax phone number for this Group is 703-308-1396.

Any inquiry of a general nature or relating to the status of this application should be directed to the Group receptionist whose telephone number is 703-305-3900.

William D. Thomson

Patent Examiner

KEVIN J. TESKA
SUPERVISORY
PATENT EXAMINER

A.U. 2123

April 19, 2001